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EXAMINER
VIGUSHIN, JOHN B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,715	OLZAK ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2827	

-- The MAILING DATE of this communication appears on the cover she t with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20-30 and 34* is/are allowed.

6)☒ Claim(s) *1,3-19 and 33* is/are rejected.

7)☒ Claim(s) *31 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The present Office Action is responsive to Applicant's Amendment filed April 01, 2004 (Certificate of Mailing date: March 29, 2004). The Examiner acknowledges the amendments to Claims 1, 6, 12, 15, 16, 17, 18, 20, 21, 25-27, 29, 30 and 32, the cancellation of Claim 2 and the addition of new Claims 33 and 34. Accordingly, Claims 1 and 3-34 are now pending in the instant amended Application.

Claim Objections

2. Claims 31 and 32 is objected to because of the following informalities:

As to Claim 31, in order to establish, clearly, the antecedent basis (appearing in amended base Claim 27) for "the printed circuit board" in line 2 of Claim 31, --parent-- should be inserted before "printed" in line 2.

As to independent Claim 32, in order to establish, clearly, the antecedent basis for "the printed circuit board" in the last two lines of the amended claim, --parent-- should be inserted before "printed" in the next-to-last line. With this correction, the last three lines of the claim provide the allowable subject matter.

Appropriate correction is required.

Rejections Based On Prior Art

3. The following references were relied upon for the rejections hereinbelow:

Tsai et al. (US 6,395,996 B1)*

Chu et al. (US 5,941,447)*

Yamaguchi et al. (US 6,147,876)*

Dalal et al. (US 5,796,591)*

*Already of record in the instant Application.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1, 3, 4, 6-14, 16-19 and 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamaguchi et al.

As to Claim 1, Yamaguchi et al. discloses: an insulating body 100D (Fig. 24) having offset first (top) and second (bottom) surfaces (Figs. 12 and 13, respectively); a plurality of surface mount (flip-chip) solder pads 131 (associated with pattern 101D and analogous to the wire-bond solder pads 107 mentioned and shown in embodiments other than the flip-chip embodiment of Figs. 24-26, the latter embodiment being the one to which the Examiner is primarily referring in the present rejection) formed on the first surface (Fig. 24; col.11: 20-26; col.13: 45-47; col.14: 2-5 and 19-22); a pattern of signal

carriers 105 communicating between the first and second surfaces (Fig. 24), each of the signal carriers 105 (specifically, metallization 105a, as shown in Fig. 7) being at least partially exposed in an area **between** the first and second surfaces (Figs. 24 and 25; col.9: 50-58; col.13: 41-45) and adjacent to the second surface (Fig. 13 shows the second surface and signal carriers 105a adjacent thereto); a plurality of electrical contacts (i.e., the contact portions continuous with signal carriers 105; Figs. 13 and 24) formed on the second surface (Fig. 13) and being electrically coupled to different ones of the signal carriers 105 (inherently so, because the electrical contacts are continuous with signal carriers 105, as indicated above), the plurality of surface mount solder pads in pattern 101D (there are **19** solder pads in pattern 101D) formed on the first surface being fewer than the plurality of electrical contacts formed on the second surface (there are **34** electrical contacts formed on the second surface continuous with the signal carriers 105 in Fig. 24; see also the less-detailed Fig. 13 which shows an exemplary second surface with the electrical contacts; the Examiner is using the more detailed Fig. 24 as the primary figure depicting the number of electrical contacts on the second surface, not shown--which is the same as the number of corresponding electrical contacts on the depicted first surface of body 100D--versus the number of surface mount solder pads in pattern 101D on the first surface); and a plurality of signal lines 109 electrically coupling one or more of surface mount solder pads 131 with predetermined ones of signal carriers 105a (Figs. 24 and 25; col.13: 48-50).

As to Claim 3, Yamaguchi et al. further discloses, in Figs. 10 and 21, insulating body 100D comprises a signal layer 116 laminated between the first and second

surfaces with one or more of the plurality of signal lines 119 (the extension of surface signal lines 109 connected thereto by vias 112) being formed on the signal layer 116 (col.9: 61-col.10: 4; col.13: 54-59).

As to Claim 4, Yamaguchi et al. further discloses each of the signal carriers 105 comprises an electrically conductive material 105a formed on an interior passage that communicates between the first and second surfaces (Figs. 7, 24 and 25; col.9: 53-58).

As to Claim 6, Yamaguchi et al. discloses: a printed circuit board (PCB) 100D (Fig. 24) having a top layer (Fig. 12) and a bottom layer (Fig. 13), and a first footprint 101D comprising a first quantity of input/output (I/O) leads 131 formed on the top layer of PCB 100D for receiving a first surface mount device 201D (Fig. 24; col.14: 19-22), and a second footprint on the bottom layer of PCB 100D (i.e., the second footprint comprising the electrical contacts formed on the bottom layer that are adjacent the edge of PCB 100D and coupled to both portions 105a and 105b of input/output lines 105, as shown in Fig. 13, said electrical contacts formed on the bottom layer being a second quantity of I/O leads greater than the first quantity of I/O leads: The second quantity of I/O leads equals **34**, as shown in Figs. 24 and 26, while the first quantity of I/O leads 131 in pattern 101D equals **19**, as shown in Fig. 24), the second footprint arranged for simulating a second surface mount device (i.e., for mounting the bottom layer, shown in Fig. 13, of PCB 100D onto the surface of motherboard 1, as shown in Fig. 26); a plurality of input/output (I/O) lines 105 connected between the first footprint 131 and one or more of a plurality of contacts corresponding to the second footprint (as discussed,

above), at least a portion of the I/O 105 adjacent to the bottom layer being exposed between the top and bottom layers (Figs. 13, 24 and 25).

As to Claim 7, Yamaguchi et al. further discloses a plurality of solder pads 131 (analogous to the wire-bond solder pads 107 mentioned and shown in embodiments other than the flip-chip embodiment of Figs. 24-26, the latter embodiment being the one to which the Examiner is primarily referring) formed on the top layer and corresponding to the first foot print 101D (Fig. 24; col.1: 20-26; col.13: 45-47; col.14: 2-5 and 19-22).

As to Claim 8, Yamaguchi et al. further discloses I/O lines 105 couple one or more of solder pads 131 on the top layer to one or more of the plurality of electrical contacts on the bottom layer (Figs. 13 and 24; col.9: 50-58; col.13: 48-50).

As to Claim 9, Yamaguchi et al. further discloses the electrical contacts further comprise a plurality of solder pads formed on the bottom layer (Fig. 13) and corresponding to the second footprint (Figs. 13, 25 and 26; col.11: 20-26; col.13: 41-45).

As to Claim 10, Yamaguchi et al. further discloses each of the plurality of I/O lines 105 further comprises a quantity of electrically conductive metal 105a deposited in a groove that communicates between the top and bottom layers (Figs. 7, 24 and 25; col.9: 53-58).

As to Claim 11, Yamaguchi et al. further discloses the second footprint is different from the first footprint (compare the second footprint defined by the electrical contacts on the bottom surface, shown in Fig. 13, with the first footprint 101D shown in Fig. 24).

As to Claim 12, Yamaguchi et al. discloses: a printed circuit board (PCB) 100D having a top layer (Fig. 12) and a bottom layer (Fig. 13); a first pattern 101D of solder pads 131 formed on the top layer of PCB 100D, the first pattern 101D being structured with a first quantity (= **19**) solder pads 131 for receiving a first surface mount device 201D (Figs. 24 and 25); a plurality of vias along a periphery of PCB 100D (Figs. 24 and 25) and communicating between the top layer and the bottom layer (Figs. 12 and 13), each of the vias having a quantity of electrically conductive material 105a deposited therein (Figs. 7, 24 and 25; col.9: 50-58; col.13: 41-45); an electrical signal line 109 coupled between one of solder pads 131 and one of the vias (Figs. 24 and 25; col.13: 48-50); and a second pattern of electrical contacts formed on the bottom layer of PCB 100D (Fig. 13) being structured with a second quantity (= **34**) of solder pads (Fig. 24) arranged to simulate a second surface mount device (i.e., for mounting the bottom layer, shown in Fig. 13, of PCB 100D onto the surface of motherboard 1, as shown in Fig. 26), the second quantity of **34** solder pads being greater than the first quantity of **19** solder pads (Fig. 24).

As to Claim 13, Yamaguchi et al. further discloses at least a portion of the electrically conductive material 105a in each of the plurality of vias adjacent to the corresponding electrical contacts formed on the bottom layer is exposed between the top and bottom layers (Figs. 13, 24 and 25).

As to Claim 14, Yamaguchi et al. further discloses each of the plurality of vias further comprises an electrically conductive material 105a plated on an interior surface of a partial cylindrical passage (Figs. 24 and 25; col.9: 53-58).

As to Claim 16, Yamaguchi et al. discloses: a body means 100D for supporting a first surface mounted device 201D relative to a printed circuit board 1 (Figs. 24, 25 and 26); a first quantity of **19** interconnecting means 131 being positioned on a first surface of body means 100D (in pattern 101D) for electrically interconnecting to a first surface mounted device 201D (col.14: 19-22); a second quantity of **34** interconnecting means, continuous with coupling means 105, being positioned on a second surface of body means 100D--i.e., the pattern of electrical contacts formed on the second (bottom) surface of body means 100D, as shown in Fig. 13 and in more detail in Fig. 24, wherein all **34** interconnecting means are continuous with the **34** coupling means 105 on both the first and second surfaces of body means 100D--for electrically interconnecting to a printed circuit board 1 structured to receive a second surface mounted device 5D (Fig. 26), the second quantity (= **34**) of interconnecting means being different from the first quantity (= **19**) of interconnecting means 131; and means 105 for electrically coupling the first and second electrically interconnecting means, at least a portion 105a of the electrically coupling means 105 being exposed between the first and second surfaces of body means 100D (Figs. 12, 13, 24 and 25; col.9: 50-58; col.13: 48-50).

As to Claim 17, Yamaguchi et al. further discloses that electrically coupling means 105 further comprises signal communication means spanning between the first and second surfaces along a peripheral surface of body means 100D (Figs. 24 and 25; col.9: 50-58).

As to Claim 18, Yamaguchi et al. further discloses the exposed portion 105a of the electrically coupling means 105 is positioned adjacent to the second (bottom) surface of body means 100D (Figs. 7 and 13; col.9: 50-58).

As to Claim 19, Yamaguchi et al. further discloses first interconnecting means 131 further comprises means for forming an electrically conductive solder joint (Fig. 24; col.11: 20-26; col.13: 45-47; col.14: 2-5 and 19-22).

As to Claim 33, Yamaguchi et al. further discloses that the second quantity of interconnecting means (= **34**) is greater than the first quantity (= **19**) of interconnecting means 131 (Fig. 24).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. in view of Dalal et al.

I. Yamaguchi et al. discloses all the limitations of the claim including signal lines 109 coupling a function of surface mount device 201D to signal carriers 105 (Fig. 25) but does not teach that signal lines 109 couple a function of a replacement surface mount device 201D to a signal carrier 105 that corresponds to a position in the pattern of signal carriers 105 that is associated with a similar function provided by a replaced

surface mount device 201D; in other words, Yamaguchi et al. does not teach that device 201D is a replacement device that has replaced a functionally similar device 201D on the surface mount solder pads 131 that are connected to said signal lines 109 that couple the function of device 201D to signal carriers 105.

II. Dalal et al. discloses replacement of surface mounted devices enabled by a surface mount device 30 having flip-chip electrode leads formed as high melting point (HMP) solder bumps 38 having low (eutectic) melting point (LMP) caps 41 that establish good electromechanical connection with the circuit board (Fig. 5; col.8: 44-57) and easy subsequent removal of the joined surface mount device for the purpose of "replacement without mechanically or thermally affecting other components on the board (col.6: 28-34).

III. Since Yamaguchi et al. teaches that the I/O leads of the first surface mounted device are flip-chip electrode leads (col.14: 19-22), and also teaches testing the surface mount multichip module 5D (by testing for defective devices 201D using second electrical interconnecting means 105) before surface mounting the module 5D to printed circuit board 1 (col.14: 26-30) and furthermore, since both Yamaguchi et al. and Dalal et al. are both in the art of solder mounting electronic components to a circuit board to form reliable electronic packages, then the concept of replacing a defective surface mount device with another of the same type of surface mount device by solder reflow and enabling such a solder-reworked replacement by fabricating the flip-chip bump leads to comprise HMP solder capped with eutectic (LMP) solder, as taught by Dalal et al., would have been readily recognized as useful for the reliable fabrication of, and

post-testing flip-chip device replacement on, the multichip modules 5D of Yamaguchi et al.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the flip-chip leads of surface mount devices 201D of Yamaguchi et al. with the flip-chip bump lead HMT/LMT structure taught by Dalal et al. in order to easily and safely replace a defective second surface mounted device 201D in Yamaguchi et al. with a known good surface mount device 201D, said defective device 201D being easily and safely removed from the module board 100D of multichip module 5D due to the flip-chip HMT/LMT bump lead structure of the surface mount devices taught by Dalal et al., and the replacement surface mount device placed on the same surface mount solder pads 131 such that the signal lines 109 couple a function of the replacement surface mount device 201D to a signal carrier 105 that corresponds to a position in the pattern of signal carriers 105 that is associated with a similar function provided by the replaced surface mount device 201D, thus enabling the multichip module 5D to perform its intended operations on system printed circuit board 1.

8. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. in view of Chu et al. and Tsai et al.

I. Yamaguchi et al. discloses PCB 100D comprises a plurality of interconnected layers including a signal layer (i.e., the conductor layers of inner layer 116 connected to signal lines 109; Fig. 10 and col.9: 66-col.10: 2).

II. Yamaguchi et al. does not explicitly teach a ground layer among the interconnected layers of PCB 100D. However, Yamaguchi et al. does teach that PCB 100D has a capacitor 122 built into the inner layers of PCB 100D and comprising conductive "plate" layers 119 and dielectric layer 126 (Fig. 23; col.12: 66-67; col.13: 5-14).

III. Chu et al. discloses, in Fig. 6, that it is old and well-known to use built-in capacitors 70 as decoupling capacitors to decouple switching noise in surface mount devices 20, 40 (col.8: 54-61; col.9: 4-10) and Tsai et al. discloses, in Figs. 2 and 4, that it is old and well-known to use built-in capacitors to suppress noise due to voltage fluctuations between the power and ground layers of a multilayer board operating at high frequencies (col.1: 15-26; col.2: 30-47; col.3: 13-18).

IV. Since Yamaguchi et al., Chu et al. and Tsai et al. all disclose a capacitor built-into a PCB carrying IC surface mount devices communicating and switching signals at high frequencies, then using the built-in capacitor 122 of Yamaguchi et al. as a decoupling capacitor for suppressing noise and ensuring the reliable functioning of the PCB and the surface mount devices thereon, as taught by Chu et al. and Tsai et al., would have been readily recognized as beneficial to the reliability of adapter comprising the PCB 100D and the surface mount devices thereon of Yamaguchi et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the conductive layers 119 of Yamaguchi et al. such that one of the conductive layers 119 is a ground layer and the other a power layer such that capacitor 122 functions as a decoupling capacitor that decouples the

switching noise from the surface mount device 201D and suppresses noise generated by high frequency voltage fluctuations between the power and ground layers 119 of the PCB 100D, as taught by Chu et al. and Tsai et al., in order to ensure reliable operation of the adapter of Yamaguchi et al.

Allowable Subject Matter

9. Claims **20**-26, 34 and **27**-30 have been allowed.

10. Claim 31 (depending from allowed base Claim 27) would be in condition for allowance if rewritten or amended to overcome the objection set forth in this Office Action.

11. Independent Claim 32 would be allowable if rewritten or amended to overcome the objection set forth in this Office action.

12. The following is a statement of reasons for the indication of allowable subject matter:

As to Claims **20**-26 and 34, patentability resides in the method resulting in the replacement of the second surface mounted device having a second quantity of I/O leads by the first surface mounted device having a first quantity of I/O leads, wherein ***the second quantity of I/O leads is different from the first quantity of I/O leads***, in combination with the other limitations of base Claim 20 *[Yamaguchi et al., as modified by Dalal et al., teach a method resulting in the replacement of a second surface mounted device having a second quantity of I/O leads by the first surface mounted*

device having a first quantity of I/O leads, wherein the second quantity of I/O leads is the same as the first quantity of I/O leads].

As to Claims **27**-31, patentability resides in *fewer of the corresponding contact areas of the foot print on the top layer of the adapter printed circuit board being provided for the replacement surface mount device than the contact areas provided on the parent printed circuit board for a replaced device*, in combination with the other limitations of base Claim 27.

As to Claim 32, patentability resides in the limitation wherein *fewer of the corresponding contact areas of the footprint are provided for the replacement device than the contact areas provided on the parent printed circuit board for the replaced device*, in combination with the other limitations of the claim.

13. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Response to Arguments

14. Applicant's arguments filed in the instant Amendment of April 01, 2004 have been fully considered but they are not persuasive regarding base Claims 1, 6, 12 and 16.

The Applicant believes that the amendments to Claims 1, 6, 12 and 16 "incorporate subject matter that the Examiner found to be allowable [in Claim 32], as recited in paragraph 11 on page 20 of the present Office Action [i.e., the Examiner's

previous Office Action of January 28, 2004]" (see p.10, the sixth and seventh paragraphs, of Applicant's Arguments in the instant Amendment). However, Applicant's assessment of the amendments to Claims 1, 6, 12 and 16 *vis-à-vis* the allowable subject matter of Claim 32 is not accurate. Claim 32 recites contact area structure on the adapter printed circuit board and contact area structure on the parent printed circuit board that conform, respectively, to the corresponding contacts of the replacement device and the device being replaced, which indirectly implies that the number of contacts on the replacement device is less than the number of contacts on the device being replaced. In contrast, Claims 1, 6, 12 and 16, as amended, now only broadly recite the structure of an adapter board with a first quantity of contact areas (i.e., a foot print) on the first surface for receiving a surface mount device, and a second quantity of contact areas on a second surface for connection to another printed circuit board, that, in combination with the other limitations of Claims 1, 6, 12 and 16, respectively, still reads on the adapter board structure and assembly disclosed by Yamaguchi et al. Nowhere in amended Claims 1, 6, 12 and 16 is it required or positively claimed that a first surface mount device is mounted to the first quantity of contacts as a replacement for a second surface mount device wherein the corresponding contact areas of the adapter board foot print that are provided for the first (i.e., replacement) device are fewer in number than the contact areas provided on the parent printed circuit board for the replaced device, along with the other necessary limitations in Claim 32, which in combination indirectly imply that the number of contacts on the replacement device is less than the number of contacts on the device being replaced, as in allowed Claim 32.

Moreover, any subsequent amendments to Claims 1, 6, 12 and 16 along the line of the allowable subject matter of Claim 32 will, at least, have to furthermore overcome the reference combination of Yamaguchi et al. in view of Dalal et al. which teaches that the replacement device has the same number of contacts as the device being replaced (see the rejection of Claim 5, above, which depends from rejected base Claim 1). Therefore, contrary to the Applicant's above-cited assertions, amended Claims 1, 6, 12 and 16 do not claim the indicated allowable subject matter of Claim 32, which must be considered in combination with all the other necessary limitation elements of Claim 32, and accordingly, have been rejected, along with their dependencies, in the present Office Action, as set forth above.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John B. Vigushin
Primary Examiner
Art Unit 2827

jbv
June 13, 2004